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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,128	09/16/2003	Ken Gary Pomaranski	200308565-1	4003

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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

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05/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/663,128	POMARANSKI ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed January 24, 2007 in response to the PTO Office Action mailed October 24, 2006. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 1, 17, 29, 35, 37, 38, 40 and 44 have been amended, and no claims have been canceled or added. Claims 1-44 remain pending in this application.

Response to Arguments

3. Applicant's arguments with respect to claims 1-44 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-44 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 17, 29, 35, 37, 38 and 44, the language "where the first memory location is less than a page of memory and where the second memory location is less than a page of memory" renders the claim indefinite. A memory location is a single address, whereas a "page of memory" is in reference to a specific size or amount of memory, or, by another interpretation, is a collection of data located at addresses. Therefore, it is unclear what is meant in relating these two concepts, because a size or amount of memory holds no bearing on a single address. For the purposes of this action, examiner will interpret any mention of a "memory location" as a range, i.e., block of memory.

Claims 2-16, 18-28, 30-34, 36 and 39-43 are rejected for being directly or indirectly dependent upon independent claims 1, 17, 29, 35 and 38, respectively, while failing to overcome their deficiencies.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 4-16, 29-30 and 32-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Wada et al (US Patent No. 6,138,257).

For claim 1, Wada discloses a system, comprising:

a memory mapping logic configured to provide access to memory locations, where the memory mapping logic can be configured to direct a memory accessing operation intended for one memory location to another memory location (the address logic of the IC device is rearranged to replace a physical space of the defective addresses with an extra or redundant address space, col. 3, lines 41-44).

a memory quality assurance logic operably connected to the memory mapping logic (a curing analysis processing section identifies defective addresses and rearranges the address logic of the IC device, col. 3, lines 39-42), where the memory quality assurance logic is configured to:

control copying contents between a first memory location and a second memory location (the curing anlysis processing section identifies defective addresses and rearranges the address logic of the IC device to replace a physical space of the defective addresses with an extra or redundant address space, col. 3, lines 39-44);

reconfigure the memory mapping logic so that memory accessing operations intended for the first memory location are directed to the second memory location (col. 3, lines 39-44); and

initiate memory testing of the first memory location (the IC testing apparatus includes a defect analysis section to perform defect analysis of the IC device concurrently with the operations by the main tester unit and curing analysis processing section, col. 3, lines 45-48),

where the first memory location is less than a page of memory and where the second memory location is less than a page of memory (the curability determining

analysis test is designed for correcting or curing failed or defective bites of the IC, col. 1, lines 57-58; the main tester unit tests an IC device for presence of a defect for each of a plurality of addresses thereof, col. 3, lines 14-16).

For claim 4, Wada discloses the memory quality assurance logic is configured to select the first memory location by one or more of, a linear method, a round-robin method, a random method, a least frequently used method, a most frequently used method, a most recently exhibiting an error method, and a least recently exhibiting an error method (the main tested unit tests an IC device for presence of a defect for each of a plurality of addresses thereof, col. 3, lines 14-16).

For claim 5, Wada discloses the memory quality assurance logic is configured to selectively logically remove the first memory location from a first set of memory by reconfiguring the memory mapping logic, based, at least in part, on a result from the memory testing of the first memory location (col. 3, lines 39-44).

For claim 6, Wada discloses the memory quality assurance logic is configured to selectively logically replace the first memory location with the second memory location by reconfiguring the memory mapping logic, based, at least in part, on a result from the memory testing of the first memory location (col. 3, lines 39-44).

For claim 7, Wada discloses the memory quality assurance logic is configured to selectively logically replace the first memory location with another memory location from a first set of memory by reconfiguring the memory mapping logic based, at least in part, on a result from the memory testing of the first memory location (col. 3, lines 39-44).

For claim 8, Wada discloses the memory quality assurance logic is configured to initiate memory testing of the first memory location by sending one or more signals to a memory testing logic (a test signal to be passed from a formatter to the pin electronics, col. 5, lines 32-33).

For claim 9, Wada discloses the memory quality assurance logic is configured to initiate memory testing of the first memory location by sending one or more signals to an onboard memory testing logic, where the onboard memory testing logic is physically connected to the first memory location (fig. 1, items 57, 62, 68, 70).

For claim 10, Wada discloses the memory quality assurance logic selects the second memory location (col. 3, lines 39-44).

For claim 11, Wada discloses the memory quality assurance logic includes one or more data stores configured to store one or more of, a memory freshness data, a memory quality data, an operating system instance to physical memory location relationship data, and a memory reconfiguration data (a main tester unit that tests an IC device for presence of a defect for each of a plurality of addresses thereof under predetermined test conditions and stores test results for individual ones of the addresses into a first memory, col. 3, lines 14-18; fig. 1, items 50, 57).

For claim 12, Wada discloses the memory quality assurance logic being operable connected to the one or more data stores (a defect analysis section that acquires, from the main tester unit, the test results for the individual addresses along with test condition data indicative of the predetermined test conditions to store the test results and the test condition data into a second memory, col. 21-26; fig. 1, items 50, 68).

For claim 13, while Wada discloses address logic is included on an IC device (col. 3, line 42; fig. 1, item 70) Wada fails to disclose the second memory location is located in internal memory of the memory mapping logic. For this feature, examiner takes Official Notice that memory mapping logics may often comprise internal memory in the form of, for example, a cache.

For claim 14, Wada discloses the second memory location is located in internal memory of the memory quality assurance logic (the curing analysis processing section identifies defective addresses on the basis of pass/fail test results mapped in the fail bit memory, col. 3, lines 39-41; fig. 1, items 50, 57).

For claim 15, Wada discloses the second memory location is physically connected to the first memory location (col. 3, lines 39-44; fig. 1, items 57, 70).

For claim 16, Wada discloses the memory quality assurance logic is configured to select the second memory location (col. 3, lines 39-41).

Claim 29 is rejected using rationale as per rejection of claim 1 above, where Wada discloses a processor (fig. 1, item 66), a memory operably connected to the processor, where the processor can access the memory (fig. 1, items 66, 67, 68, 69).

For claim 30, Wada discloses the system is embedded in a computer (the invention may be imnplemented as a recording medium storing a program executable by a computer or by one or more CPUs for carrying out such an IC testing method, col. 4, lines 26-29).

Claim 32 is rejected using rationale as per rejection of claims 11 and 29 above.

Claim 33 is rejected using rationale as per rejection of claims 12 and 29 above.

For claim 34, Wada discloses a memory location selection logic configured to select the first memory location and the second memory location (col. 3, lines 39-44; a data selector of the pin control section comprises a memory having stored therein various test signal creating data, such as address data and to-be-written data, switching signal creating data and expected value data, col. 5, lines 58-60).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al (US Patent No. 6,138,257) in view of Van Doren (US PGPub No. 20010037435).

For claim 2, while Wada discloses a fail memory and an input/output switching section for use with the invention, Wada fails to disclose the memory mapping logic includes a crossbar.

Van Doren helps disclose multiprocessor building blocks as nodes interconnected by a switch fabric, such as a hierarchical switch, where each node comprises address mapping and routing logic that includes a routing table, and the hierarchical switch may be implemented as a crossbar switch (par. 0014).

Wada and Van Doren are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Van Doren suggests that it would have been desirable to incorporate crossbar switching into the system of Wada because this would help in the application of a distributed address mapping and routing technique that supports flexible configuration and partitioning in a modular multiprocessor system having a plurality of multiprocessor building blocks interconnected by a switch fabric (par. 0011). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Wada as suggested by Van Doren to incorporate the feature as claimed.

For claim 3, Wada fails to disclose the memory mapping logic includes one or more address translation tables.

Van Doren helps disclose each node comprises address mapping and routing logic that includes a routing table (par. 0014).

Wada and Van Doren are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Van Doren suggests that it would have been desirable to incorporate the use of an address translation table into the system of Wada because address translation mapping in conjunction with source routing would help provide a flecible configuration and partitioning in a modular multiprocessor system having a plurality of multiprocessor building blocks interconnected by a switch fabric (par. 0011). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Wada as suggested by Van Doren to incorporate the feature as claimed.

10. Claims 17-25, 28, 35-37 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al (US Patent No. 6,138,257) in view of Leung et al (US PGPub No. 20050044467).

For claim 17, Wada discloses a method comprising:

selectively copying contents of a first memory location to a second memory location (col. 3, lines 39-44);

logically replacing the first memory location with the second memory location (col. 3, lines 39-44); and

initiating memory testing of the first memory location (col. 3, lines 45-48),

where the first memory location is less than a page of memory and where the second memory location is less than a page of memory (col. 1, lines 57-58; col. 3, lines 14-16).

Wada fails to disclose initiating memory testing without an operating system interaction.

Leung helps disclose a memory system with transparent error correction circuitry, abstract; from the outside of the memory, the ECC storage and logic are completely transparent (par. 0016).

Wada and Leung are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Leung suggests that it would have been desirable to incorporate memory testing that is transparent to an operating system into the system of Wada because this allows for efficient error-

correction in an embedded environment (par. 0008). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Wada as suggested by Leung to incorporate the feature as claimed.

For claim 18, Wada and Leung disclose access to the contents of the first memory location as copied to the second memory location can continue concurrently with the memory testing (Wada: col. 3, lines 45-48).

For claim 19, Wada and Leung disclose the memory testing of the first memory location can continue without consuming a non-memory operating system resource (Leung: par. 0008).

Claim 20 is rejected using rationale as per rejection of claims 4 and 17 above.

Claim 21 is rejected using rationale as per rejection of claims 5 and 17 above.

Claim 22 is rejected using rationale as per rejection of claims 5 and 17 above.

For claim 23, Wada and Leung disclose selectively logically replacing the first memory location with a third memory location, where the first memory location and the third memory location are physically located in the same memory apparatus (Wada: col. 3, lines 39-44; fig. 1, items 57, 70).

For claim 24, Wada and Leung disclose providing a report concerning a quality of the first memory location, where the report is based, at least in part, on the testing of the first memory location (Wada: col. 3, lines 14-18; fig. 1, items 50, 57).

For claim 25, Wada and Leung disclose storing a quality data associated with the quality of the first memory location, where the quality data is based, at least in part, on the testing of the first memory location (Wada: col. 21-26; fig. 1, items 50, 68).

Claim 28 is rejected using rationale as per rejection of claims 16 and 17 above.

Claim 35 is rejected using rationale as per rejection of claims 17 and 22, where Wada discloses the invention may be implemented as a recording medium storing a program executable by a computer or by one or more CPUs for carrying out such an IC testing method (col. 4, lines 26-29).

Claim 36 is rejected using rationale as per rejection of claims 17 and 21.

Claim 37 is rejected using rationale as per rejection of claims 17 and 22 above, where Wada discloses the invention may be implemented as a recording medium storing a program executable by a computer or by one or more CPUs for carrying out such an IC testing method on an IC (col. 4, lines 26-29).

Claim 44 is rejected using rationale as per rejection of claims 17 and 36 above.

11. Claims 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al (US Patent No. 6,138,257) in view of Leung et al (US PGPub No. 20050044467) and further in view of Nakamura (US Patent No. 6,523,135).

For claim 26, while Wada and Leung disclose predetermined test conditions such as a predetermined test speed and pattern (col. 7, lines 14-16), where a pattern generating section generates a specific test pattern (col. 1, lines 25-31), Wada and Leung fail to disclose testing the first memory location includes two or more test methods.

Nakamura helps disclose a built-in self-test circuit for a memory including a test mode controller, abstract; including its own microprocessor for generating test patterns

such as column bars, checker board, marching, shifted diagonal test and other test patterns (col. 1, lines 15-18).

Wada, Leung and Nakamura are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Nakamura suggests that it would have been desirable to incorporate two or more test methods into the combined system of Wada and Leung because this would help to test substantially all the functions or any desired functions of a memory (col. 2, lines 24-25). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined system of Wada and Leung as suggested by Nakamura to incorporate the feature as claimed.

For claim 27, while Wada and Leung disclose predetermined test conditions such as a predetermined test speed and pattern (col. 7, lines 14-16), where a pattern generating section generates a specific test pattern (col. 1, lines 25-31), Wada and Leung fail to disclose the first memory location can be tested by one or more of, a parity test, an electrical test, a striping test, a marching one test, a marching zero test, and a pattern test.

Nakamura helps disclose a built-in self-test circuit for a memory including a test mode controller, abstract; including its own microprocessor for generating test patterns such as column bars, checker board, marching, shifted diagonal test and other test patterns (col. 1, lines 15-18).

Wada, Leung and Nakamura are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Nakamura suggests

that it would have been desirable to incorporate two or more test methods into the combined system of Wada and Leung because this would help to test substantially all the functions or any desired functions of a memory (col. 2, lines 24-25). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combined system of Wada and Leung as suggested by Nakamura to incorporate the feature as claimed.

12. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wada et al (US Patent No. 6,138,257) in view of Mellor et al (US PGPub No. 20040169885).

For claim 31, Wada fails to disclose the system is embedded in an image forming device.

Mellor helps disclose a method embodiment for memory management in which print job data is stored in the memory of an image forming device (par. 0001-0002).

Wada and Mellor are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. Mellor suggests that it would have been desirable to incorporate an image forming device into the system of Wada because this allows the processing of a print job and producing of an image such as text and/or graphics on a media sheet (par. 0020). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Wada as suggested by Mellor to incorporate the feature as claimed.

Allowable Subject Matter

13. Claims 38-43 are objected to as being dependent upon a rejected base claim or rejected for deficiencies under 35 U.S.C. 112, second paragraph, but would be allowable if rewritten to fix all said deficiencies and in independent form, including all of the limitations of the base claim and any intervening claims.

Contact Information

14. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

HONG CHONG Kim
PRIMARY EXAMINER

4-29-07